In the Specification:

The paragraph starting on page 1 line 20 and ending on page 2, line 2 now reads as:

The prior art discloses various rotational speed sensors which are intended to be able to detect the revolutions of a wheel. By way of example, a sensor with a gearwheel is known, in which the teeth and gaps of the gearwheel are converted into logic H=HIGH and L=LOW states, respectively. The teeth and the gaps of the gearwheel are formed as alternating magnetic north and south poles of a ring magnet. When the gearwheel is rotated, a magnetic sensor, e.g. a Hall sensor, senses the alternating sequence of north and south poles. This alternating sequence can be then converted into logic H=HIGH and L=LOW states, respectively, of a magnet signal. In the case of a prior art two-wire current interface, these states are output such that each state is assigned a specific current consumption. As a result, the two supply lines can simultaneously be used as signal output lines as well.

The paragraph starting on page 8, line 5 and ending on page 8, line 8 now reads as:

Figs. 3A and 3B are signal diagrams illustrating, with respect to time, signal magnitudes of the circuit according to Fig. 1,

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wherein Fig. 3A represents the known measurement mode and Fig. 3B illustrates the changeover to the communication mode;

The paragraph starting on page 8, line 10 and ending on page 8, line 12 now reads as:

Figs. 4A, 4B, and 4C are signal diagrams illustrating the transmitted signal pulses in an embodiment of the method according to the invention; and

a3 [Insert, between line 12 and line 14 on page 8, the following:]

-- Fig. 5 shows a circuit for recognizing the presence of a negative resistance and for switching the sensor from normal operation to test mode or communication mode. --

Insert, between line 14 and line 16 on page 11, the following:

-- A circuit for recognizing the presence of a negative resistance and for switching the sensor from normal operation to test mode or communication mode is shown in Fig. 5. The circuit of Fig. 5 uses the output signal of a comparator "volt_hi", which indicates the supply voltage level V_i (volt_hi=HI corresponds to a high supply voltage V_i, and LO corresponds to a low supply voltage V_i). In addition, the circuit of Fig. 5 uses the output signal of the sensor

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"curr_hi", which corresponds to the sensor current I_s, (curr_hi=HI corresponds to a high current, and LO to a low current). A negative resistance is present when "volt_hi" and "curr_hi" are both HI or both LO at the same time.

The circuit of Fig. 5 does not show the comparator, which distinguishes between the high and low levels of the supply voltage V_i to provide a digital "volt_hi" with HI- and LO-levels. Preferably, the comparator includes a hysteresis, i.e., a forbidden gap between the high and low levels to detect large voltage changes.

(Cont'd)

The circuit of Fig. 5 checks whether or not the digital data generator operates with a negative resistance characteristic for a given number of "curr_hi" pulses. If so, the "OPEN_OUT" signal is activated to switch the sensor from the normal operation to the test mode or communication mode. The check for the negative resistance is performed by the INV, NAND, OR and AND gates, which provide a HI-level to the reset-input of the counter when the resistance is negative and a LO-level to the reset-input of the counter when the resistance is positive. The other input of the counter (clock-input) is connected with the "curr_hi"-signal, which increments the counter from zero to five for each curr_hi" cycle as long as the reset-input of the counter is at HI-level. Once the counter has been incremented to "5", it activates the "

OPEN_OUT" signal to switch the sensor into the test or communication mode. Further, the counter remains at "5" until the reset-input is returned to LO-level due to a measured positive resistance at the input of the circuit of Fig. 5 (LO-level at the reset-input). When the reset-input returns to LO-level, the counter is reset to "0".

The shift register in Fig. 5 serves to mask possible time periods during which the processor of the digital data generator does not have time to initiate the correct "volt_hi" level (processor delay). Without the shift register, short "wrong" volt_hi/curr_hi signals (i.e., HI/LO or LO/HI) would interrupt each negative resistance pulse sequence and, accordingly, the output signal "OPEN_OUT" would never be activated. To suppress the "wrong" volt_hi/curr_hi signals, the shift register of Fig. 5 generates on each pulse slope a short time window during which the NAND and OR gates are deactivated. Master clock signal "mcl" and slave clock signal "scl" serve to clock the shift register. If "wrong" signals are detected outside the short time window, the reset-input returns to LO-level, the counter is reset to zero and the " OPEN_OUT" signal is deactivated. The same can be achieved with a central reset signal "rq" which resets the shift register and the counter. --

(C4 (Cont'd)